## REMARKS

This application has been reviewed in light of the Final Office Action mailed September 28, 2005. Reconsideration of this application in view of the below remarks is respectfully requested. Claims 1-64 are pending in the application with Claims 1, 7, 18, 21, 26, 27, 32, 42 and 45 being in independent form.

### I. Rejection of Claims 1-64 Under 35 U.S.C. §102(e)

Claims 1-64 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,654,270 issued to Osaka et al. In response, Applicant respectfully traverses the rejection with respect to Claims 1-64 for at least the reasons provided below.

Osaka et al. teaches memory modules using directional coupling (i.e. crosstalk) to communicate between a memory module and a plurality of memory chips. Applicant clearly claims usage of data wiring and not directional coupling to communicate between the memory controller and memory chips. In fact, the only reference to either directional coupling or crosstalk is found in paragraph 0249 (page 55, line 26 through page 56, line 5) referring to FIG. 33. Paragraph 0249 discloses phase shifting write and read data phase signals by two clocks to avoid crosstalk. Therefore, crosstalk, in the case of the present disclosure, is detrimental to the operation of the system, while removal of the directional coupling in Osaka et al. would render that system inoperable for its stated purpose.

The Examiner has misinterpreted Applicant's claimed "at least one buffer connected to the controller via a plurality of data wiring for data transmission" to be analogous to the Osaka et al. disclosed buffers 6-2 and 5-1 in module 2-1 of FIG. 4. As, shown, the module 2-1 buffers are connected to the memory controller by way of internal data wiring and to memory circuits by way of directional coupling.

However, Claim 1 specifically defines the placement of the claimed "at least one buffer" as being mounted on a module with a plurality of memory chips. Additionally, Applicant's claimed buffer is connected to the controller via a plurality of data wiring and connected to the plurality of memory circuits via a plurality of internal data wiring in the module. Therefore, it is clear that the buffers of Osaka et al. are not connected to the memory controller and memory circuits as recited in Applicant's limitations.

The buffers 6-2 and 5-1 of module 2-2 are mounted on a module with a plurality of memory chips 10-2 – 10-9, while module 2-1 does not contain any memory chips at all. Therefore, the proper analog for the claimed at least one buffer is buffers 6-2 and 5-1 in module 2-2 of FIG. 4.

The buffers 6-2 and 5-1 of module 2-2 are clearly shown in FIG.1-5 and 12-14 to require directional coupling in order to transmit data to the module containing the memory controller. Thus, the Osaka disclosed buffers 6-2 and 5-1 of module 2-2 are not connected to the controller via a plurality of data wiring.

Further, Applicant's Claimed data wiring connecting the controller with the buffer in the memory module is adapted to transmit data at a higher speed than the internal wiring connecting the buffer to the memory circuits inside the memory module. However, Osaka et al. only discloses that data can be transmitted via directional coupling at a high speed when return-to-zero (RTZ) signals are converted to non-return-to-zero (NRZ) signals. Therefore, there is no indication that this high speed is of a higher speed than the data transfer speed of the internal data wiring.

It is well-settled by the Courts that "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the

claim." Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick Company, et al., 730 F.2d 1452, 221 USPQ 481 (Fed. Cir., 1984). Therefore, as demonstrated above, because Osaka et al. does not disclose each and every element recited in the present claims, Applicant respectfully submits that the rejection has been traversed.

Moreover, because Osaka et al. states that directional coupling is the "conventional" method of data transmission in the art, there is clearly no suggestion or teaching in Osaka et al. of data transmission via data wiring as recited in Applicant's claims.

Therefore, for at least the reasons given above, Claims 1-64 are believed patentably distinct and allowable over Osaka et al. Accordingly, Applicant respectfully requests withdrawal of the rejection, with respect to Claims 1-64 under 35 U.S.C. §102(e).

## CONCLUSIONS

In view of the foregoing remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-64 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Applicant's undersigned attorney at the number indicated below.

Respectfully submitted,

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